REMARKS

In the office action, the Examiner (1) rejected Claim 8 under 35 U.S.C. § 112, second paragraph, as being indefinite, (2) rejected Claims 1-5, 7-9, 17-21, 23, 24 and 26-30 under 35 U.S.C. § 103(a) as being unpatentable over "Applicants' Admitted Prior Art (AAPA) in view of U.S. Patent No. 6,211,608 issued to Raina et al. ("Raina"), U.S. Patent No. 5,534,743 issued to Jones et al. ("Jones '743"), and U.S. Patent No. 6,069,443 et al. ("Jones '443"), (3) rejected Claims 6, 22 and 31 under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Raina, Jones '743, Jones '443 and further in view of U.S. Patent No. 5,578,896 issued to Haung et al. ("Haung"). Reconsideration and allowance of the application, as amended, are requested.

I. § 112 Rejection

The Examiner initially rejected Claim 8 as being indefinite. Claim 8 has been amended to specify that the substrate comprises glass to correct an obvious error. No new matter is added.

II. § 103(a) Rejections

The Examiner rejected Claims 1-5, 7-9, 17-21, 23, 24 and 26-30 under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view Raina, Jones '743, and Jones '443. The Examiner states that the AAPA differs from the claimed invention in that a separately deposited insulator layer is disposed between the resistive layer and the dielectric structure. The Examiner contends that Raina discloses that resistive layers tend to have pinholes causing shorts to develop, and teaches the formation of a buffer layer insulator to substantially eliminate the possibility of short circuiting via the resistive layer. The Jones references are cited for disclosing that multiple insulative layers can be used to avoid short circuiting due to pin hole defects. These rejections are respectfully traversed.

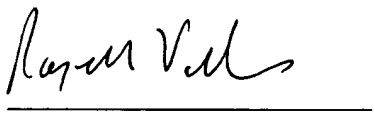
Raina discloses an FED having a buffer layer 58 between an overlying resistor layer 60 and an underlying cathode conductive layer 56 (as shown in Fig. 8 of the reference). The buffer layer 58 is used so that pinhole defects that extend through the resistor layer 60 terminate at the buffer layer 58 without reaching the cathode conductive layer 56. Accordingly, the buffer layer 58 is positioned between the resistor layer and the cathode conductive layer 56. In addition, the buffer layer 58 completely covers the top and sides of the cathode conductive layer 56 tht face the resistor layer 60.

Claim 1 of the present application is directed to a method of making a cathode assembly of an FED, which includes forming an emitter electrode structure on the substrate; forming a resistive layer over the emitter electrode structure; and forming an insulative layer on a portion of the resistive layer. Thus, an insulative layer is formed on a portion of a resistive layer, which in turn is formed over the emitter electrode structure. As indicated in the specification (e.g., on page 8) a significant purpose of the insulative layer is to reduce the possibility of shorting between the addressing column line and the row line structure, which shorting might result, e.g., from intrinsic defects in the dielectric structure or unintended variations in spacing between the substrate and grid surfaces. By contrast, Raina only discloses a buffer layer positioned between the resistor layer and the cathode conductive layer 56. It does not suggest placing the buffer layer on the resistor layer because that would defeat the purpose of the buffer layer, which is to protect the cathode conductive structure from pin holes in the resistor layer. Therefore, even assuming that AAPA is properly combinable with Raina, the combination would, at best, only teach that a buffering layer be placed between the emitter electrode structure on the substrate and the resistive layer on the emitter electrode structure of AAPA. One skilled in the art would find no suggestion or have any incentive for placing the buffering layer on a portion of the resistive layer. That, in fact, would defeat the purpose of the buffering layer, which is to protect the cathode conductive structure from pin holes in the resistor layer as noted above. Thus, the cited

prior art teaches away from the combination suggested by the Examiner. The cited Jones and Huang references add nothing further in this regard. Therefore, Claim 1 and dependent Claims 2-9 are patentable over the cited references. The remaining pending claims are similarly allowable.

Claims 1-9, 17-24 and 26-31 are pending in the present application. As the application is now believed to be in condition for allowance, issuance of a Notice of Allowance is respectfully requested.

Respectfully submitted,



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